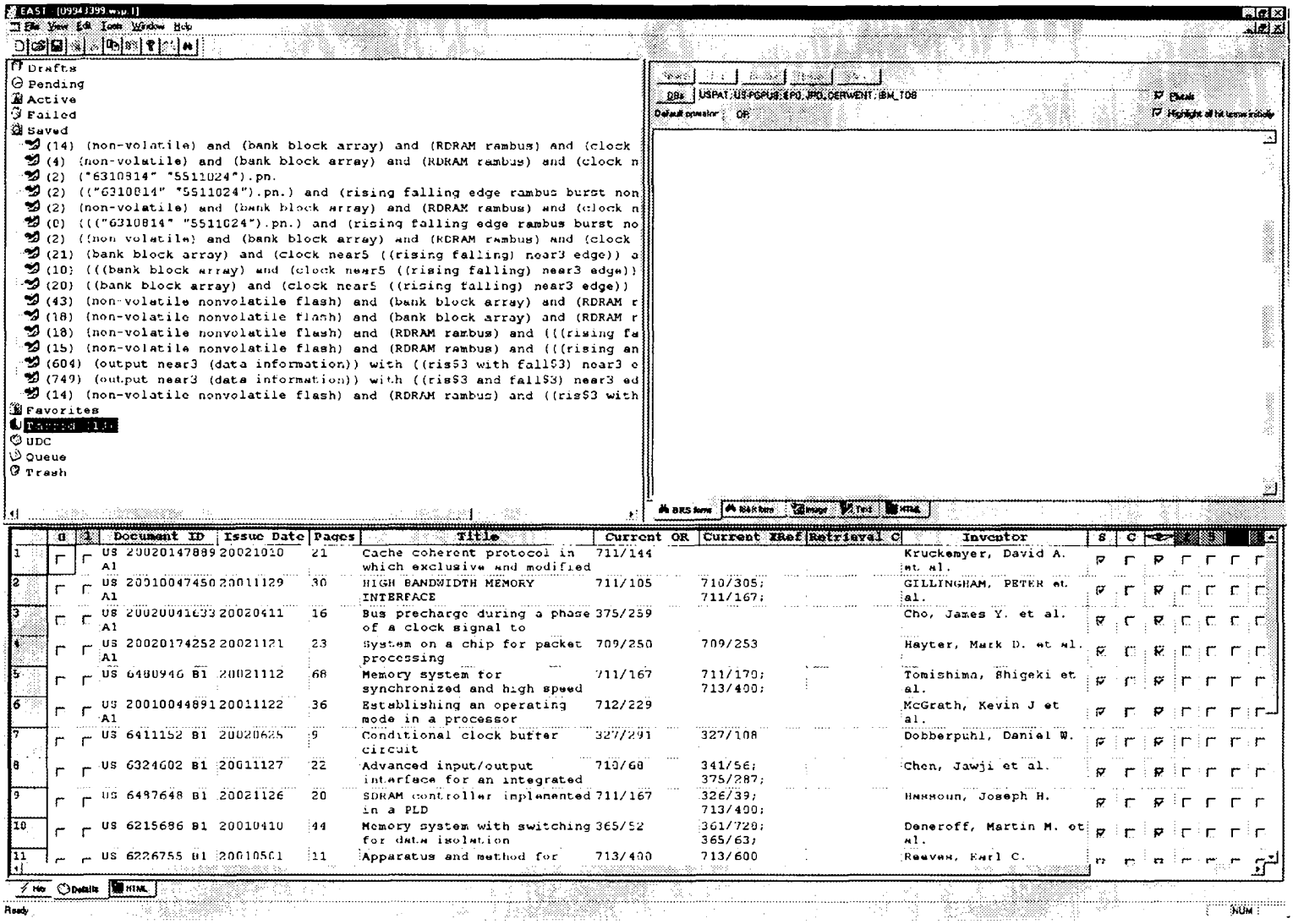

	G	L	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C					
1	☐	☐	US 20020147889 A1	20021010	21	Cache coherent protocol in which exclusive and modified	711/144			Kruckemyer, David A. et al.	☑	☐	☑	☐	☐	☐	☐
2	☐	☐	US 20010047450 A1	20011129	30	HIGH BANDWIDTH MEMORY INTERFACE	711/105	710/305; 711/167;		GILLINGHAM, PETER et al.	☑	☐	☑	☐	☐	☐	☐
3	☐	☐	US 20020041633 A1	20020411	16	Bus precharge during a phase of a clock signal to	375/259			Cho, James Y. et al.	☑	☐	☑	☐	☐	☐	☐
4	☐	☐	US 20020174252 A1	20021121	23	System on a chip for packet processing	709/250	709/253		Hayter, Mark D. et al.	☑	☐	☑	☐	☐	☐	☐
5	☐	☐	US 6480946 B1	20021112	68	Memory system for synchronized and high speed	711/167	711/170; 713/400;		Tomishima, Shigeki et al.	☑	☐	☑	☐	☐	☐	☐
6	☐	☐	US 20010044891 A1	20011122	36	Establishing an operating mode in a processor	712/229			McGrath, Kevin J et al.	☑	☐	☑	☐	☐	☐	☐
7	☐	☐	US 6411152 B1	20020625	9	Conditional clock buffer circuit	327/291	327/108		Dobberpuhl, Daniel W.	☑	☐	☑	☐	☐	☐	☐
8	☐	☐	US 6324602 B1	20011127	22	Advanced input/output interface for an integrated	710/60	341/56; 375/287;		Chen, Jawji et al.	☑	☐	☑	☐	☐	☐	☐
9	☐	☐	US 6487648 B1	20021126	20	SDRAM controller implemented in a PLD	711/167	326/39; 713/400;		Hashoun, Joseph H.	☑	☐	☑	☐	☐	☐	☐
10	☐	☐	US 6215686 B1	20010410	44	Memory system with switching for data isolation	365/52	361/720; 365/63;		Deneroff, Martin M. et al.	☑	☐	☑	☐	☐	☐	☐
11	☐	☐	US 6226755 B1	20010501	11	Apparatus and method for	713/400	713/600		Reeves, Earl C.	☐	☐	☐	☐	☐	☐	☐